PATENT
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
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Moo Jin LEE et al.	)	Confirmation No.: 1841
	)	
Application No.: 10/673,542	)	Group Art Unit: 2629
	)	
Filed: September 30, 2003	)	Examiner: Ke Xiao
	)	
For: METHOD AND APPARATUS FOR SUPPLY OF POWER SOURCE IN LIQUID CRYSTAL DISPLAY	)	**Mail Stop Appeal Brief**

Mail Stop Appeal Brief
Commissioner of Patents
U.S. Patent and Trademark Office
Alexandria, VA 22314

Sir/Madam:

APPELLANT'S BRIEF UNDER 37 C.F.R. § 41.37

This brief is in furtherance to the Notice of Appeal filed in the above-identified patent application on July 15, 2009. A fee of $540.00 required under 37 C.F.R. §41.20(b)(2) is being filed concurrently herewith. The period for filing this brief extends through October 15, 2009, with a petition for a one-month extension of time.

1. The Real Party in Interest

The real party in interest in this appeal is LG Display, Ltd. of Republic of Korea.

2. Related Appeals and Interferences

Appellant is not aware of any other appeals or interferences that will directly affect, or be directly affected by, or have a bearing on the Board's decision in this appeal.

3. Status of Claims

The status of the claims is as follows upon filing of this Appeal Brief:

Claims canceled: 1-4, 6-17, 19, 21, 23-26, and 28-31.
Claims withdrawn from consideration but not canceled: None
Claims pending: 5, 18, 20, 22, 27, and 32.
Claims objected to: None
Claims allowed: None
Claims rejected: 5, 18, 20, 22, 27, and 32.

The claims on appeal are 5, 18, 20, 22, 27, and 32.

4. The Status of Amendments

Appellant filed an Amendment under 37 C.F.R. § 1.116 on June 4, 2009. The Advisory Action mailed June 17, 2009, indicated that the Amendment under 37 C.F.R. § 1.116 was entered and an explanation of how the new or amended claims would be rejected was provided.

5. Summary of Claimed Subject Matter

Aspects of Appellant's present invention relate generally to a liquid crystal display (LCD) and methods for supplying power to LCD devices. The present invention, as summarized below, is described in detail at paragraphs [0034]-[0057] of the specification with reference to Figures 3-9 and 10-13.

In accordance with the exemplary embodiment of the invention of independent claim 5, a method for supplying a power to a liquid crystal display is provided. The method comprises taking a power source voltage having a constant level of less than 2.9V from a power source of a system (see, for example, paragraphs [0036]-[0039] and [0049]-[0051]); supplying the power source voltage having the constant level of less than 2.9V to an interface circuit (see, for example, paragraphs [0039] and [0049]), a timing controller (see, for example, paragraphs [0038] and [0051]), a data driving circuit (see, for example, paragraphs [0036] and [0049]) and a gate driving circuit (see, for example, paragraphs [0037] and [0050]) for processing digital signal; and raising or reducing the power source voltage having the constant level of less than 2.9V using a DC-DC converter to generate a reference voltage VDD, a common voltage VCOM, gamma voltages GMA1~10, a gate high voltage VGH and a gate low voltage VGL (see, for example, paragraphs [0040] and [0053]), wherein the reference voltage VDD, the common voltage VCOM and the gamma voltages GMA1~10 are supplied to the data driving circuit, and the gate high voltage VGH and the gate low voltage VGL are supplied to the gate driving circuit (see, for example, paragraphs [0041] and [0053]).

In accordance with the exemplary embodiment of the invention of independent claim 18, an apparatus for supplying a power to a liquid crystal display is provided. The apparatus comprises a power source of a system for generating a power source voltage having a constant level under 2.9V (see, for example, paragraphs [0036]-[0039] and [0049]-[0051]); an interface circuit (see, for example, paragraphs [0039] and [0049]), a timing controller (see, for example, paragraphs [0038] and [0051]), a data driving circuit (see, for example, paragraphs [0036] and [0049]) and a gate driving circuit (see, for example, paragraphs [0037] and [0050]) used to process the digital signal by taking the power source voltage; and a DC-DC converter for raising or reducing the power source voltage having the constant level under 2.9V to generate a reference voltage VDD, a common voltage VCOM, gamma voltages GMA1~10, a gate high voltage VGH and a gate low voltage VGL, wherein the reference voltage VDD, the common voltage VCOM and the gamma voltages GMA1~10 are supplied to the data driving circuit, and the gate high voltage VGH and the gate low voltage VGL are supplied to the gate driving circuit (see, for example, paragraphs [0040] and [0053]), wherein the power source voltage having the constant level under 2.9V is supplied to the interface circuit, the timing controller, the data driving circuit and the gate driving circuit (see, for example, paragraphs [0041] and [0053]).

In accordance with the exemplary embodiment of the invention of dependent claim 20, an apparatus for supplying a power to a liquid crystal display is provided. In the apparatus, the interface circuit receives a synchronous signal, a clock signal and digital video data from the system (see, for example, paragraph [0035]); the timing controller controls the data driving circuit and the gate driving circuit by using the synchronous signal and the clock signal from the

interface circuit (see, for example, paragraph [0035]), and the data driving circuit supplies the digital video data to the liquid crystal panel and the gate driving circuit supplies a scan pulse to the liquid crystal panel (see, for example, paragraph [0035]).

In accordance with the exemplary embodiment of the invention of independent claim 22, a method for supplying a power to a liquid crystal display is provided. The method comprises providing a first power source voltage from a power source of a system wherein the first power source voltage is 3.3V (see, for example, paragraph [0035]); generating a second power source voltage having a constant level of less than 2.9V from the first power source voltage of 3.3V using a reducing circuit (see, for example, paragraphs [0042]-[0047]); supplying the second power source voltage having the constant level of less than 2.9V to the interface circuit (see, for example, paragraphs [0039] and [0049]), the timing controller (see, for example, paragraphs [0038] and [0051]), the data driving circuit (see, for example, paragraphs [0036] and [0049]), and the gate driving circuit (see, for example, paragraphs [0037] and [0050]) for processing digital signal of the interface circuit, the timing controller, the data driving circuit, and the gate driving circuit; generating a reference voltage VDD, a common voltage VCOM, gamma voltages GMA1~10, a gate high voltage VGH and a gate low voltage VGL from the first power source voltage of 3.3V using a DC-DC converter (see, for example, paragraphs [0040] and [0053]); and supplying the reference voltage VDD, the common voltage VCOM and the gamma voltages GMA1~10 to the data driving circuit and supplying the gate high voltage and the gate low voltage to the gate driving circuit (see, for example, paragraphs [0041] and [0053]).

In accordance with the exemplary embodiment of the invention of independent claim 27, a method for supplying a power to a liquid crystal display is provided. The method comprises providing a power source voltage from a power source of a system wherein the power source voltage has a constant level of less than 2.9V (see, for example, paragraphs [0036]-[0039] and [0049]-[0051]); supplying the power source voltage having the constant level of less than 2.9V to the interface circuit (see, for example, paragraphs [0039] and [0049]), the timing controller (see, for example, paragraphs [0038] and [0051]), the data driving circuit (see, for example, paragraphs [0036] and [0049]) and the gate driving circuit (see, for example, paragraphs [0037] and [0050]); generating a reference voltage VDD, a common voltage VCOM, gamma voltages GMA1~10, a gate high voltage VGH and a gate low voltage VGL from the power source voltage having the constant level of less than 2.9V using a DC-DC converter (see, for example, paragraphs [0040] and [0053]); and supplying the reference voltage VDD, the common voltage VCOM and the gamma voltages GMA1~10 to the data driving circuit and supplying the gate high voltage and the gate low voltage to the gate driving circuit (see, for example, paragraphs [0041] and [0053]).

In accordance with the exemplary embodiment of the invention of independent claim 32, a method for supplying a power to a liquid crystal display is provided. The method comprises providing a first power source voltage from a system wherein the first power source voltage is 3.3V (see, for example, paragraph [0035]); supplying the first power source voltage of 3.3V to the data driving circuit and the gate driving circuit for processing digital signal of the data driving circuit and the gate driving circuit (see, for example, FIGs. 3, 4 and 11, and the

description about the gate driving and the data driving circuit); generating a second power source voltage having a constant level of less than 2.9V from the first power source voltage of 3.3V using a reducing circuit (see, for example, paragraphs [0042]-[0047]); supplying the second power source voltage having the constant level of less than 2.9V to the interface circuit (see, for example, paragraphs [0039] and [0049]) and the timing controller (see, for example, paragraphs [0038] and [0051]) for processing digital signal of the interface circuit and the timing controller; generating a reference voltage VDD, a common voltage VCOM, gamma voltages GMA1~10, a gate high voltage VGH and a gate low voltage VGL from the first power source voltage of 3.3V using a DC-DC converter (see, for example, paragraphs [0040] and [0053]); and supplying the reference voltage VDD, the common voltage VCOM and the gamma voltages GMA1~10 to the data driving circuit and supplying the gate high voltage and the gate low voltage to the gate driving circuit (see, for example, paragraphs [0041] and [0053]).

6. Grounds of Rejection to be Reviewed on Appeal

Claims 5, 18, 20, 22, 27, and 32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Appellant's Admitted Prior Art (AAPA) and *Tsutsui* (US 7,196,701).

7. Argument

The Rejection under 35 U.S.C. § 103(a) over AAPA and *Tsutsui*

Appellant respectfully asserts that the rejection under 35 U.S.C. § 103(a) is improper and should be reversed for at least the following reasons.

The Final Office Action dated March 16, 2009 alleges that "[a] person of ordinary skill in the art upon analyzing *Tsutsui* would have reasonably used any voltage values that are appropriate for different loads, including voltages less than 2.9V. The exact voltage values used are dependent on the voltage that is required to drive the load and are completely arbitrary, and therefore it would have been obvious to try voltages less than 2.9V along with low power loads to achieve the predictable result of power conservation," (emphasis added). The Advisory Action dated June 17, 2009 admits that "[p]rior art fails to teach 2.9V but instead teaches 3.0V." Nevertheless, the Advisory Action further alleges that "one of ordinary skill in the art would have been motivated to use any voltage value in (sic) that satisfies the circuitry in question" and that "the difference of 0.1V for supplying power to IC is a complete matter of obvious design choice," (emphasis added). Appellant understands the Examiner to be alleging that the voltages that are supplied to the (1) interface circuit, the (2) timing controller, the (3) data driving circuit and the (4) gate driving circuit can be optimized by routine experimentation. Appellant respectfully disagrees.

MPEP § 2144.05 states that "[a] particular parameter must first be recognized as a result-effective variable, i.e., a variable which achieves a recognized result, before the determination of the optimum or workable ranges of said variable might be characterized as routine experimentation. *In re Antonie*, 559 F.2d 618, 195 USPQ 6 (CCPA 1977)." The Examiner failed to establish that *all four voltages*, i.e., the voltages that are supplied to the (1) interface circuit, the (2) timing controller, the (3) data driving circuit and the (4) gate driving circuit, are

result-effective variables. Accordingly, the Final Office Action failed to establish a *prima facie* case of obviousness.

In view of the foregoing, Appellant respectfully asserts that the rejections of independent claims 5, 18, 22, 27, and 32 are improper. Moreover, Appellant respectfully asserts that dependent claim 20 is allowable at least because of its dependency from independent claim 18 and the reasons set forth above. Thus, Appellant respectfully requests the reversal of the Examiner's rejections and the allowance of the pending claims. If there are any other fees due in connection with the filing of this Appellant's Brief, please charge the fees to our Deposit Account No. 50-0310.

If a fee is required for an extension of time under 37 C.F.R. §1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account No. 50-0310.

Respectfully submitted,

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/Wonjoo Suh/

By: _____
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8. Claims Appendix

The claims on appeal read as follows:

Claims 1-4 (Canceled).

Claim 5 (Previously Presented) A method for supplying a power to a liquid crystal display, comprising the steps of:

taking a power source voltage having a constant level of less than 2.9V from a power source of a system;

supplying the power source voltage having the constant level of less than 2.9V to an interface circuit, a timing controller, a data driving circuit and a gate driving circuit for processing digital signal; and

raising or reducing the power source voltage having the constant level of less than 2.9V using a DC-DC converter to generate a reference voltage VDD, a common voltage VCOM, gamma voltages GMA1~10, a gate high voltage VGH and a gate low voltage VGL, wherein the reference voltage VDD, the common voltage VCOM and the gamma voltages GMA1~10 are supplied to the data driving circuit, and the gate high voltage VGH and the gate low voltage VGL are supplied to the gate driving circuit.

Claims 6-17 (Canceled).

Claim 18 (Previously Presented) An apparatus for supplying a power to a liquid crystal display comprising:

a power source of a system for generating a power source voltage having a constant level under 2.9V;

an interface circuit, a timing controller, a data driving circuit and a gate driving circuit used to process the digital signal by taking the power source voltage; and

a DC-DC converter for raising or reducing the power source voltage having the constant level under 2.9V to generate a reference voltage VDD, a common voltage VCOM, gamma voltages GMA1~10, a gate high voltage VGH and a gate low voltage VGL, wherein the reference voltage VDD, the common voltage VCOM and the gamma voltages GMA1~10 are supplied to the data driving circuit, and the gate high voltage VGH and the gate low voltage VGL are supplied to the gate driving circuit,

wherein the power source voltage having the constant level under 2.9V is supplied to the interface circuit, the timing controller, the data driving circuit and the gate driving circuit.

Claim 19 (Canceled)

Claim 20 (Previously Presented) The apparatus for supplying a power to a liquid crystal display according to claim 18, wherein the interface circuit receives a synchronous signal, a clock signal and digital video data from the system; and

the timing controller controls the data driving circuit and the gate driving circuit by using the synchronous signal and the clock signal from the interface circuit,

wherein the data driving circuit supplies the digital video data to the liquid crystal panel and the gate driving circuit supplies a scan pulse to the liquid crystal panel.

Claim 21 (Canceled).

Claim 22 (Previously Presented) A method for supplying a power to a liquid crystal display, having an interface circuit, a timing controller, a data driving circuit, and a gate driving circuit for processing digital signal, comprising the steps of:

providing a first power source voltage from a power source of a system wherein the first power source voltage is 3.3V;

generating a second power source voltage having a constant level of less than 2.9V from the first power source voltage of 3.3V using a reducing circuit;

supplying the second power source voltage having the constant level of less than 2.9V to the interface circuit, the timing controller, the data driving circuit, and the gate driving circuit for processing digital signal of the interface circuit, the timing controller, the data driving circuit, and the gate driving circuit;

generating a reference voltage VDD, a common voltage VCOM, gamma voltages GMA1~10, a gate high voltage VGH and a gate low voltage VGL from the first power source voltage of 3.3V using a DC-DC converter; and

supplying the reference voltage VDD, the common voltage VCOM and the gamma voltages GMA1~10 to the data driving circuit and supplying the gate high voltage and the gate low voltage to the gate driving circuit.

Claim 23-26 (Canceled)

Claim 27 (Previously Presented) A method for supplying a power to a liquid crystal display, having an interface circuit, a timing controller, a data driving circuit, and a gate driving circuit for processing digital signal, comprising the steps of:

providing a power source voltage from a power source of a system wherein the power source voltage has a constant level of less than 2.9V;

supplying the power source voltage having the constant level of less than 2.9V to the interface circuit, the timing controller, the data driving circuit and the gate driving circuit;

generating a reference voltage VDD, a common voltage VCOM, gamma voltages GMA1~10, a gate high voltage VGH and a gate low voltage VGL from the power source voltage having the constant level of less than 2.9V using a DC-DC converter; and

supplying the reference voltage VDD, the common voltage VCOM and the gamma voltages GMA1~10 to the data driving circuit and supplying the gate high voltage and the gate low voltage to the gate driving circuit.

Claim 28-31 (Canceled)

Claim 32 (Previously Presented) A method for supplying a power to a liquid crystal display, having an interface circuit, a timing controller, a data driving circuit, and a gate driving circuit for processing digital signal, comprising the steps of:

providing a first power source voltage from a system wherein the first power source voltage is 3.3V;

supplying the first power source voltage of 3.3V to the data driving circuit and the gate driving circuit for processing digital signal of the data driving circuit and the gate driving circuit;

generating a second power source voltage having a constant level of less than 2.9V from the first power source voltage of 3.3V using a reducing circuit;

supplying the second power source voltage having the constant level of less than 2.9V to the interface circuit and the timing controller for processing digital signal of the interface circuit and the timing controller;

generating a reference voltage VDD, a common voltage VCOM, gamma voltages GMA1~10, a gate high voltage VGH and a gate low voltage VGL from the first power source voltage of 3.3V using a DC-DC converter; and

supplying the reference voltage VDD, the common voltage VCOM and the gamma voltages GMA1~10 to the data driving circuit and supplying the gate high voltage and the gate low voltage to the gate driving circuit.

9. **Evidence Appendix**

No information is appended under this section.

10. Related Proceedings Appendix

No information is appended under this section.